IN THE CLAIMS

Please amend the claims as follows.

1-35. (Canceled)

36. (Previously Presented) A method for accessing an asynchronously-accessible dynamic random access memory, comprising:

receiving an external row address to the asynchronously-accessible dynamic random access memory;

selecting between a burst mode and a pipelined mode of operation of the asynchronously-accessible dynamic random access memory;

selecting between a read operation and a write operation of the asynchronously-accessible dynamic random access memory; and

obtaining a first external column address for accessing the asynchronously-accessible dynamic random access memory.

37. (Previously Presented) The method, as in Claim 36, further comprising:

obtaining a second external column address subsequent to the first external column address for operation in the pipelined mode.

38. (Previously Presented) The method, as in Claim 36, further comprising:

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

39. (Previously Presented) The method, as in Claim 36, further comprising:

selecting at least one address pathway based on the selection between the burst mode and the pipelined mode.

40-58. (Canceled)

59. (Previously Presented) A method of accessing a memory, comprising:

receiving an external row address;

choosing whether the memory is in a burst mode of operation or in a pipeline mode of operation;

selecting a read operation or a write operation for the memory; and

executing a read or write operation in the chosen mode of operation.

60. (Previously Presented) The method of claim 59, and further comprising:

switching between the burst mode of operation and the pipelined mode of operation.

61. (Previously Presented) The method of claim 59, and further comprising:

switching between the read operation and the write operation.

62. (Previously Presented) The method of claim 59, wherein the operations are performed in a different order.

63. (Previously Presented) A method of accessing a memory, comprising:

receiving an external row address;

selecting a burst mode of operation or a pipeline mode of operation of the memory;

selecting a read operation or a write operation for the memory;

selecting an external address only data path, obtaining an external column address, and obtaining information from the memory if the read operation of the pipeline mode of operation is selected;

selecting an external address only data path, obtaining an external column address, and providing information to the memory if the write operation of the pipeline mode of operation is selected;

selecting an initial buffered external address data path, obtaining an initial external column address, obtaining information from the memory, and generating internal column addresses and obtaining further information from the memory until all desired internal column addresses are used if the read operation of the burst mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an initial external column address, providing information to the memory, and generating internal column addresses and providing further information to the memory until all desired internal column addresses are used if the write operation of the burst mode of operation is selected.

64. (Previously Presented) The method of claim 63, wherein the operations are performed in a different order.

65. (Previously Presented) A method of operating a memory circuit, comprising:

receiving a mode select signal;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between active and inactive;

generating an internal address on a cycle of the second enabling signal based on the initial external address;

changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state; and

receiving an external address on each cycle of the second enabling signal.

66. (Previously Presented) A method for accessing a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between inactive and active;

generating an internal address on a cycle of the second enabling signal based on the initial external address; and

switching the mode of operation to a pipeline mode on successive cycles of the second enabling signal by changing the mode select signal.

67. (Previously Presented) A method for operating a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;

selecting a read operation or a write operation of the memory;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

changing the mode select signal to select a pipeline mode of operation.

68. (Currently Amended) A method for data transfer direction selection in a memory, comprising:

selecting a read or a write operation of the memory;

selecting a burst or a pipeline mode of operation for the memory;

selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an ~~inital~~ initial external column address, accessing the memory, and generating internal column addresses when the burst mode of operation is selected.

69. (Previously Presented) A storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode;

selection circuitry for selecting between a read operation and a write operation;

an external column address data path for pipeline read and write operation column address retrieval;

an internal column address generation module for burst read and write operation column address generation; and

pipelined/burst circuitry coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the storage device in either mode.

70-74. (Canceled)

75. (Previously Presented) A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory operation selected from a group consisting of a read operation and a write operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

76. (Previously Presented) The method of claim 75, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

77. (Previously Presented) The method of claim 75, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

78. (Previously Presented) The method of claim 75, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation;

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

79. (Previously Presented) The method of claim 78, further comprising:

selecting at least one address pathway based on subsequently switching to the burst mode of operation.

80. (Previously Presented) A method for accessing an asynchronously-accessible dynamic random access memory (DRAM), comprising:

receiving an external row address to the asynchronously-accessible DRAM;

switching from a burst mode of operation to a pipelined mode of operation;

selecting a memory read operation; and

obtaining a first external column address for accessing the asynchronously-accessible DRAM.

81. (Previously Presented) The method of claim 80, further comprising:

obtaining a second external column address subsequent to obtaining the first external column address for operation in the pipelined mode.

82. (Previously Presented) The method of claim 80, further comprising:

selecting at least one address pathway based on switching to the pipelined mode of operation.

83. (Previously Presented) The method of claim 80, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation; and

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.